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EXAMINER	
AHMED, SALMAN	

ART UNIT	PAPER NUMBER
2419	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,129	LOUGHRAN ET AL.	
	Examiner	Art Unit	
	SALMAN AHMED	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8,9,11,14-17,19-23,26 and 29-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4-6, 8, 9, 11, 14-17, 19-23, 26 and 29-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 2, 4, 5, 8, 11, 15-17 19, 20, 23, 26 and 29-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wybenga et al. (US2004/0223504, hereinafter Wybenga) in view of Willis (US PAT PUB 20050201387).

Regarding claims 1, Wybenga et al. disclose a plurality of nodes interconnected through a fabric (paragraphs 0035, routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-speed switch fabrics 155a and 155b), at least one node (see paragraph 35 line 6 routing nodes) comprising a plurality of network processing devices (see figure 2 box 230 classification processor box 240 system

processor box 250 async variables controller, Network Processor 260), at least one network processing device for receiving digital information, for determining a destination within the node for the digital information, and for providing the digital information to the destination (see paragraph 21 line 5-15); a shared bus structure for coupling each of the network processing devices with each other (see paragraph 40 line 3 PCI bus and figure 2 ref 290, where figure 2 box 230 classification processor box 240 system processor box 250 async variables controller, Network Processor 260 are coupled to each other using bus 290. Network Processor 260 is coupled to rest of the mentioned processor using bus 290 via PCI Bridge 270); and an interface (see figure 2 box 280 GBE which interfaces figure 1 box 150 switch fabric) for coupling the at least one processing devices with the fabric (see figure 2 box 280 GBE interconnects with box 260 network processor wherein 280 GBE which interfaces figure 1 box 150 switch fabric) to support communication between nodes (paragraphs 0035, routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-speed switch fabrics 155a and 155b, figure 2, 280 GBE).

Wybenga does not explicitly teach a node supports native transport of digital information to and from a fabric in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information; wherein each at least one network processing device supports routing and forwarding of digital information within corresponding nodes in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information.

Willis in the same or similar field of endeavor teaches a node supports native transport of digital information to and from a fabric in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information; wherein each at least one network processing device supports routing and forwarding of digital information within corresponding nodes in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information (abstract, paragraph 0056, 0058, a communication node contains intelligence for directing both internet protocol (IP) packets and Asychronous Transfer Mode (ATM) cells toward their destinations. The ATM cells and IP packets may be received within a common data stream. The respective devices process the ATM cells and IP packets to direct the cells and packets to the proper output ports towards their destinations. The device is capable of performing policing and quality of service (QOS) processing on both the ATM cells and the IP packets. FIG. 7 provides a functional diagram that exhibits the lifetime of processing from input to output for a given data stream in the illustrative embodiment. The OC-48 input data stream 90 is first demultiplexed 92 into the separate tributaries (also known as "channels"). The data within each of the channels is decapsulated 94 to remove the data from SONET frames and layer 2 frames. ATM input processing 96 is performed on ATM cells in the input data and IP input processing 98 is performed on IP packets in the input data. Data passes over the interconnect 62 to an output line card. The output line card performs output processing 102, which includes queuing and traffic shaping 102. Encapsulation 104 is performed on the data and the respective tributaries

are multiplexed 106 to produce an OC-48 output data stream 108. he resulting data in the respective tributaries may be in any of a number of different formats. The receive ASIC 70 delineates this data (step 112 in FIG. 8) to gain access to the ATM cells, PPP frames or FR frames carried therein (see 94 in FIG. 7). Each IP packet may be composes of multiple ATM cells or may be contained in a PPP frame or FR frame).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate in Wybenga's system/method the steps of a node supporting native transport of digital information to and from a fabric in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information; wherein each at least one network processing device supports routing and forwarding of digital information within corresponding nodes in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information as suggested by Willis. The motivation is that (as suggested by Willis, paragraph 0005) such method provides a device that not only can perform IP packet forwarding and routing but can also perform ATM switching and routing; the device allows a network developer to not commit exclusively to a single protocol; rather the device allows the developer to support a number of different protocols within a single device; thus making the network more efficient. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

Regarding claim 2, Wybenga et al. teaches the destination is determined in response to at least one of stored routing rules and characteristics of the corresponding digital information (see paragraph 39 line 14 classification processor).

Regarding claim 4, Wybenga et al. implicitly teaches each at least one network processing device supports routing and forwarding of cell information and packet information simultaneously (see paragraph 46).

Wybenga does not explicitly teach each at least one network processing device supports routing and forwarding of cell information and packet information simultaneously.

Willis in the same or similar field of endeavor teaches each at least one network processing device supports routing and forwarding of cell information and packet information simultaneously (abstract, paragraph 0056, 0058, a communication node contains intelligence for directing both internet protocol (IP) packets and Asychronous Transfer Mode (ATM) cells toward their destinations. The ATM cells and IP packets may be received within a common data stream. The respective devices process the ATM cells and IP packets to direct the cells and packets to the proper output ports towards their destinations. The device is capable of performing policing and quality of service (QOS) processing on both the ATM cells and the IP packets. FIG. 7 provides a functional diagram that exhibits the lifetime of processing from input to output for a given data stream in the illustrative embodiment. The OC-48 input data stream 90 is first demultiplexed 92 into the separate tributaries (also known as "channels"). The data within each of the channels is decapsulated 94 to remove the data from SONET frames

and layer 2 frames. ATM input processing 96 is performed on ATM cells in the input data and IP input processing 98 is performed on IP packets in the input data. Data passes over the interconnect 62 to an output line card. The output line card performs output processing 102, which includes queuing and traffic shaping 102. Encapsulation 104 is performed on the data and the respective tributaries are multiplexed 106 to produce an OC-48 output data stream 108. he resulting data in the respective tributaries may be in any of a number of different formats. The receive ASIC 70 delineates this data (step 112 in FIG. 8) to gain access to the ATM cells, PPP frames or FR frames carried therein (see 94 in FIG. 7). Each IP packet may be composes of multiple ATM cells or may be contained in a PPP frame or FR frame).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate in Wybenga's system/method the steps of each at least one network processing device supports routing and forwarding of cell information and packet information simultaneously as suggested by Willis. The motivation is that (as suggested by Willis, paragraph 0005) such method provides a device that not only can perform IP packet forwarding and routing but can also perform ATM switching and routing; the device allows a network developer to not commit exclusively to a single protocol; rather the device allows the developer to support a number of different protocols within a single device; thus making the network more efficient. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market

forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

Regarding claim 5, Wybenga et al. teaches the at least one network processing device directly delivers the routed digital information into a memory of the destination (see paragraph 36 line 5-10).

Regarding claim 8, Wybenga et al. teaches the interface comprises a System Interface (see figure 142 PMD module) and a it Maintenance Interface (see paragraph 41 line 8 doorbell register interface).

Regarding claim 11, Wybenga et al. teaches the node further comprises: a general-purpose processor in operative communication with the shared bus structure (see paragraph 41 line 6-16 and figure 2 box 240 system processor) for at least one of controlling the plurality of network processing devices of the corresponding node and performing maintenance on the corresponding node (see paragraph 42).

Regarding claim 15, Wybenga et al. teaches interface comprises at least one external system input/output interface supporting at least one transport mechanism type (see figure 1 box 146 IOP).

Regarding claim 16, Wybenga et al. teaches the at least one transport mechanism type comprising at least one of Asynchronous Transfer Mode, Internet Protocol, and Frame Relay (see paragraph 36 line 13- 14).

Regarding claim 17, Wybenga et al. teaches a communication node comprising: a plurality of network processing devices (see figure 2 box 230 classification processor box 240 system processor box 250 async variables controller, Network Processor 260)

at least one network processing device for receiving digital information (see figure 2 box 230 classification processor box 240 system processor box 250 async variables controller), for determining a destination within the node for the digital information, and for providing the digital information to the destination (see paragraph 21 line 5-15), the destination determined in response to at least one of stored routing rules and characteristics of the corresponding digital information (see paragraph 39 line 14 classification processor); a shared bus structure for coupling each of the network processing devices with each other (see paragraph 40 line 3 PCI bus and figure 2 ref 290, where figure 2 box 230 classification processor box 240 system processor box 250 async variables controller, Network Processor 260 are coupled to each other using bus 290. Network Processor 260 is coupled to rest of the mentioned processor using bus 290 via PCI Bridge 270); and a System Interface (see figure 2 box 280 Gbe which interfaces with figure 1 box 150 switch fabric) and at least one of a Maintenance Interface (see paragraph 41 doorbell register interface where a doorbell interrupt is initiated when a device performs a write operation to a pre-defined Configuration Data Register. This interrupt can be enabled and disabled. Thus provide maintenance through an interface) and an external system input/output interface coupled to at least one network processing device (see figure 2 box 280 GBE interconnects with box 260 network processor wherein 280 GBE which interfaces figure 1 box 150 switch fabric, figure 2, 280 GBE and two sided arrow connecting PCI bridge 270 to network processor 260).

Wybenga does not explicitly teach a communication node supports native transport of digital information to and from other nodes of a communication network in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information; wherein each at least one network processing device supports routing and forwarding of digital information within the communication node in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information.

Willis in the same or similar field of endeavor teaches a communication node supports native transport of digital information to and from other nodes of a communication network in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information; wherein each at least one network processing device supports routing and forwarding of digital information within the communication node in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information (abstract, paragraph 0056, 0058, a communication node contains intelligence for directing both internet protocol (IP) packets and Asychronous Transfer Mode (ATM) cells toward their destinations. The ATM cells and IP packets may be received within a common data stream. The respective devices process the ATM cells and IP packets to direct the cells and packets to the proper output ports towards their destinations. The device is capable of performing policing and quality of service (QOS) processing on both the ATM cells and

the IP packets. FIG. 7 provides a functional diagram that exhibits the lifetime of processing from input to output for a given data stream in the illustrative embodiment. The OC-48 input data stream 90 is first demultiplexed 92 into the separate tributaries (also known as "channels"). The data within each of the channels is decapsulated 94 to remove the data from SONET frames and layer 2 frames. ATM input processing 96 is performed on ATM cells in the input data and IP input processing 98 is performed on IP packets in the input data. Data passes over the interconnect 62 to an output line card. The output line card performs output processing 102, which includes queuing and traffic shaping 102. Encapsulation 104 is performed on the data and the respective tributaries are multiplexed 106 to produce an OC-48 output data stream 108. he resulting data in the respective tributaries may be in any of a number of different formats. The receive ASIC 70 delineates this data (step 112 in FIG. 8) to gain access to the ATM cells, PPP frames or FR frames carried therein (see 94 in FIG. 7). Each IP packet may be composes of multiple ATM cells or may be contained in a PPP frame or FR frame).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate in Wybenga's system/method the steps of a communication node supports native transport of digital information to and from other nodes of a communication network in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information; wherein each at least one network processing device supports routing and forwarding of digital information within the communication node in a plurality of network protocols, including network protocols for transporting cell information and network

protocols for transporting packet information as suggested by Willis. The motivation is that (as suggested by Willis, paragraph 0005) such method provides a device that not only can perform IP packet forwarding and routing but can also perform ATM switching and routing; the device allows a network developer to not commit exclusively to a single protocol; rather the device allows the developer to support a number of different protocols within a single device; thus making the network more efficient. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

Regarding claims 19, 20, 23 and 26 and Wybenga et al. disclose all the limitations as discussed in the rejection of claims 4, 5, 11 and (14 and 15) are therefore claims 19, 20, 23 and 26 are rejected using the same rationales.

Regarding claims 33, Wybenga et al. disclose a digital communication system, comprising: a plurality of communication nodes interconnected through an interconnect fabric (paragraphs 0035, routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-speed switch fabrics 155a and 155b), at least one communication node comprising: a plurality of network processing devices (see figure 2 box 230 classification processor box 240 system processor box 250 async variables controller, Network Processor 260); a shared bus structure coupling the plurality of network processing devices with each other (see paragraph 40 line 3 PCI bus and figure 2 ref 290, where figure 2 box 230 classification processor box 240 system processor box 250 async variables controller, Network Processor 260 are coupled to

each other using bus 290. Network Processor 260 is coupled to rest of the mentioned processor using bus 290 via PCI Bridge 270); and a plurality of interfaces, at least one interface (see figure 2 box 280 GBE which interfaces figure 1 box 150 switch fabric) coupling at least one network processing device with the interconnect fabric (see figure 2 box 280 GBE interconnects with box 260 network processor wherein 280 GBE which interfaces figure 1 box 150 switch fabric) to support communication with other communication nodes of the plurality of communication nodes (paragraphs 0035, routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-speed switch fabrics 155a and 155b, figure 2, 280 GBE); wherein the at least one network processing device receives digital information from the plurality of interfaces and the plurality of network processing devices (see figure 2 box 230 classification processor box 240 system processor box 250 async variables controller), determines a destination for the digital information, and provides the digital information to the determined destination (see paragraph 21 line 5-15 and see paragraph 39 line 14 classification processor).

Wybenga does not explicitly teach communication node supports native transport of digital information to and from the interconnect fabric in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information; wherein each at least one network processing device supports routing and forwarding of digital information within corresponding communication nodes in a plurality of network protocols, including

network protocols for transporting cell information and network protocols for transporting packet information.

Willis in the same or similar field of endeavor teaches communication node supports native transport of digital information to and from the interconnect fabric in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information; wherein each at least one network processing device supports routing and forwarding of digital information within corresponding communication nodes in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information (abstract, paragraph 0056, 0058, a communication node contains intelligence for directing both internet protocol (IP) packets and Asychronous Transfer Mode (ATM) cells toward their destinations. The ATM cells and IP packets may be received within a common data stream. The respective devices process the ATM cells and IP packets to direct the cells and packets to the proper output ports towards their destinations. The device is capable of performing policing and quality of service (QOS) processing on both the ATM cells and the IP packets. FIG. 7 provides a functional diagram that exhibits the lifetime of processing from input to output for a given data stream in the illustrative embodiment. The OC-48 input data stream 90 is first demultiplexed 92 into the separate tributaries (also known as "channels"). The data within each of the channels is decapsulated 94 to remove the data from SONET frames and layer 2 frames. ATM input processing 96 is performed on ATM cells in the input data and IP input processing 98 is performed on IP

packets in the input data. Data passes over the interconnect 62 to an output line card. The output line card performs output processing 102, which includes queuing and traffic shaping 102. Encapsulation 104 is performed on the data and the respective tributaries are multiplexed 106 to produce an OC-48 output data stream 108. he resulting data in the respective tributaries may be in any of a number of different formats. The receive ASIC 70 delineates this data (step 112 in FIG. 8) to gain access to the ATM cells, PPP frames or FR frames carried therein (see 94 in FIG. 7). Each IP packet may be composes of multiple ATM cells or may be contained in a PPP frame or FR frame).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate in Wybenga's system/method the steps of communication node supports native transport of digital information to and from the interconnect fabric in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information; wherein each at least one network processing device supports routing and forwarding of digital information within corresponding communication nodes in a plurality of network protocols, including network protocols for transporting cell information and network protocols for transporting packet information as suggested by Willis. The motivation is that (as suggested by Willis, paragraph 0005) such method provides a device that not only can perform IP packet forwarding and routing but can also perform ATM switching and routing; the device allows a network developer to not commit exclusively to a single protocol; rather the device allows the developer to support a number of different protocols within a single device; thus making the network more efficient. Known work in

one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

In regards to claims 29, 31 and 35 Wybenga does not explicitly teach network processing device supports routing and forwarding of cell information and packet information in parallel.

Willis in the same or similar field of endeavor teaches network processing device supports routing and forwarding of cell information and packet information in parallel (see figure 7).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate in Wybenga's system/method the steps of network processing device supports routing and forwarding of cell information and packet information in parallel as suggested by Willis. The motivation is that (as suggested by Willis, paragraph 0005) such method provides a device that not only can perform IP packet forwarding and routing but can also perform ATM switching and routing; the device allows a network developer to not commit exclusively to a single protocol; rather the device allows the developer to support a number of different protocols within a single device; thus making the network more efficient. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

In regards to claims 30, 32, 34 and 36, Wybenga does not explicitly teach node/network processing device supports native transport of cell information and packet information simultaneously.

Willis in the same or similar field of endeavor teaches node/network processing device supports native transport of cell information and packet information simultaneously (see figure 7).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate in Wybenga's system/method the steps of node/network processing device supports native transport of cell information and packet information simultaneously as suggested by Willis. The motivation is that (as suggested by Willis, paragraph 0005) such method provides a device that not only can perform IP packet forwarding and routing but can also perform ATM switching and routing; the device allows a network developer to not commit exclusively to a single protocol; rather the device allows the developer to support a number of different protocols within a single device; thus making the network more efficient. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

4. Claims 6, 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wybenga et al. and Willis as applied to claims 1 and 17 above and further in view of background of Wybenga.

Regarding claims 6, 14 and 21, Wybenga et al. in view of Willis disclose all the subject matter of the claimed invention with the exception of the at least one network processing device supports peer-to-peer routing within corresponding nodes.

Wybenga et al. background from the same or similar fields of endeavor teaches the use of new services, such as voice-over-IP (VoIP) or streaming applications, and the development of mobile Internet (see Wybenga et al. background paragraph 2) which are forms of peer-to-peer system.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the new services, such as voice-over-IP (VoIP) or streaming applications, and the development of mobile Internet as taught by the background of Wybenga et al. in apparatus and method for workflow-based routing in a distributed architecture router of Wybenga et al. and Willis in order to provide peer-to-peer system service and system transmission method. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

5. Claims 9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wybenga et al. and Willis as applied to claims 1 and 17 above and further in view of Oner (US2005/0078696).

Regarding claims 9 and 22, Wybenga et al. teaches the interface comprises at least one of a System Interface (see figure 142 PMD module) and a Maintenance

Interface (see paragraph 41 line 8 doorbell register interface), and disclose all the subject matter of the claimed invention with the exception of the interface comprises a multiplexer for creating a multiplexed stream from the Digital information.

Oner from the same or similar fields of endeavor teaches the use of address multiplexer (see Oner paragraph 125 line 9 and figure 9 box 92 address multiplexer).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the address multiplexer as taught by Oner in apparatus and method for workflow-based routing in a distributed architecture router of Wybenga et al. and Willis in order to enhance the efficiency of the system. Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art.

Response to Arguments

6. Applicant's arguments see pages 9-13 of the Remarks section, filed 2/23/2009, with respect to the rejections of the claims have been fully considered and are moot in view of new ground of rejections presented in this office action.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SALMAN AHMED whose telephone number is (571)272-8307. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Salman Ahmed/

Examiner, Art Unit 2419